REHDESIGN

HGT

Hercules Grafics Terminal

Manual

1. Introduction

The *REHDESIGN* HGT is a complete terminal on an Euro-Card, designed for use in standard ECB-bus based micro-computer systems. The HGT performs communication between the computer and the user by displaying output data on the screen and accepting keyboard input from the user. The interface to the computer (host) is a parallel bus interface with very high transfer rates. As a pure slave device, the HGT is passive on the bus and therefore should be usable in all ECB-bus based computers. As keyboard, a common PC/AT-compatible MF-2 keyboard is used; the monitor is of standard Hercules-type (monochrome, with TTL signals).

2. Circuit Details

The heart of the HGT is the Z80 microprocessor (IC1), which controls the complete terminal board. Its memory address space consists of program memory, data memory, and screen memory, while the parallel bus interface, a general purpose input (GPI) port, the CRTC control registers, and a general purpose output port (GPO) are accessed as I/O devices. The CRTC (cathode ray tube controller) is contained within the HGC (hercules grafics controller).

On power-up, the Z80 is reset by IC5 (TL 7705). If chosed by the jumper J1, the HGT can also be reset by the reset signal of the ECB bus system. The processor clock is generated by an integrated oscillator and is directly fed to the CPU.

Decoding of the memory- and I/O-addresses is done by two decoder chips (IC2 & IC9, both '139). Always one half of the decoder chip is used to generate the select signals for the HGC, while the other half decodes the select signals for the other devices.

The program memory of the Z80 consists of a single EPROM chip (IC3), which is addressed in the first 16 KB of the memory address space. If more than 16 KB of program memory is needed, so-called page mode EPROMs may be used. With these types, always one 16 KB page out of several is selected by "writing" the page number to the EPROM area. If less memory is needed, it's also possible to use 8 KB chips without circuit changes.

Data memory is made of a 32 KB static RAM (IC4). Since the address area for the RAM is only 16 KB, the physical memory is divided in two banks, which can be switched by I/O accesses. For this, one of the GPO bits is used.

The 64 KB screen memory (IC13, IC14) also is split in two banks of 32 KB, which are accessed in the remaining CPU address area. Switching between the two banks is again done by a GPO bit. Accesses to the screen memory are generally done via the HGC, which constantly accesses that memory for screen refresh and enables CPU accesses only during display pauses. If necessary, the HGC "freezes" the CPU access by asserting the WAIT signal, until the screen memory is accessible again.

The HGC has 20 address lines, by which it receives the accessed address from the CPU. The addresses of screen memory and CRTC registers are decoded internally, following the PC standard. The screen memory is from 0B0000h to 0BFFFFh, and the CRTC registers are from 3B4h to 3BFh (with these decoding, the HGC chip can be directly connected to the expansion bus in PC systems). Since the upper four address lines aren't needed during I/O accesses, they can be fixed to the appropriate values needed for memory accesses. This way, all memory select signals reaching the HGC will force accesses. To avoid false selections when A15 is low (program & data memory), the HGC memory select signals are only generated if A15 is high. I/O addressing is not critical, since the Z80 directly supports 16-Bit I/O addresses.

For the HGC, the W86855 was chosen. It has an internal character set ROM and therefore can be used even without external font EPROM. However, since it also supports external character sets, the HGT allows for an EPROM containing up to four fonts. Switching between internal and external fonts, and selecting one of the four external fonts, are realised with GPO bits.

The HGC has its own crystal oscillator, providing the pixel clock and all video timing signals. Thus, it is totally asynchronous to the CPU. The video signals are output to the monitor directly from the HGC which has the appropriate drivers on chip.

The bus interface for communication with the host is made of two 8-bit registers (IC7,8) and a GAL (IC6). By appropriate programming of the GAL it functions as a bidirectional, parallel interface. For the host, it looks exactly like a Z80-SIO: two I/O addresses are used, one for the data register, and one for the status register. Of the status register, only two bits are used (buffer free / character available). The status signals on the terminal side are available as hardware signals. Incoming characters from the host cause an interrupt of the Z80, while the output status can be read as another GPI bit.

Connection of an MF2-keyboard requires two bidirectional open-collector I/O lines. In the HGT, these are realised by two bits of the GPI and GPO each, with the GPO signals converted to open-collector type by two transistors. The clock signal causes an NMI (non-maskable interrupt) at the Z80 for each bit, so the terminal is able to react on keyboard actions at every time. There are two connector options for the keyboard: you may use a PCB-mounted 6-contact Mini-DIN socket (compatible to PS/2), or connect to a standard 5-contact DIN socket by short wires (for this, all keyboard signals are also available at a 5-pin single-inline header).

The GPI and GPO ports are made of IC10 and IC11. These ports are used for simple I/O functions. The input port (IC10) reads the keyboard signals, host interface status, and five jumpers which could be used for configuration options. The output port (IC11) controls font switching and selection, bank switching for data and screen memory, keyboard signal outputs, and speaker.

For connection of a speaker, an open-collector signal is available at a 3-pin header. The other two pins carry power supply and ground, so any small speaker or electronic circuit can be connected. If a speaker is connected, the generation of audible frequencies must be done by software.

3. Parts List

IC1	Z80 CPU, CMOS, 6 MHz
IC2,IC9	74 HCT 139
IC3	27 C 64/128/513
IC4	43256
IC5	TL 7705
IC6	GAL 20 V 8, 25 ns or faster
IC7	74 HCT 574
IC8	74 ACT 574
IC10	74 HCT 245
IC11	74 HCT 259
IC12	W 86855
IC13,IC14	4464 (resp. 41464)
IC15	27 C 64/128
IC16	74 HCT 08
T1-T3	BC 547 or equivalent
C1,C2	22 p ker. RM 5
C3	100 n RM 5

C4		1 µ Ta. RM 2.5
C5,C6		120 p ker. RM 5
CK1-10,CK14-17		14x 100 n ker. RM 5
CK11-13		3x 10 µ Ta. RM 2.5
R1		4 k 7
R2,R3		2 k 2
R4,R5,R6,R7		22 R
R8,R9,R10		10 k
R11		1 k
RN1		RSIL 8x 10k
Q1		16 MHz HC-18U
QOS1		4 / 6 MHz, CMOS
CN1	ECB	VME-type connector 64-pin ac
CN2	KEY	Mini-DIN 6-pin, or Header 1x5
CN3	VIDEO	DE-9 S 90°
CN4	BEEP	Header 1x3
J1	RESET	Header 1x3
J2-6	USER	Header (Configuration Jumpers)

4. Jumper Settings

Jumper J1 (Reset) normally is in the "upper" position, so that the bus signal "Reset Out" (26c) causes a reset of the terminal, too. The configuration jumpers J2 to J6 are not currently used by the terminal software and thus can be left open.

5. GAL Programming

With the GAL of the type 20V8 (IC6) all control and decoding functions of the parallel bus interface are realised:

```
TITLE       HGT ECB-IF GAL IC6
AUTHOR      TILMANN REH
COMPANY     REHDESIGN
DATE        06.08.1992

CHIP HGT PALCE20V8

ba0 ba3 ba4 ba1 rd ba5 ba6 ba7 host wr biorq gnd
brd bwr bd2 ttxe /trxf bd0 brp twp trp bwp ba2 vcc;

STRING baseadr '(/ba7 * ba6 * ba5 * /ba4 * /ba3 * /ba2 * /ba1)' ; 60h

EQUATIONS

; For both sides accesses, M1 need not be considered, since /RD and /WR are
; fully decoded (and both are inactiv during interrupt acknowledge).

; Register read and write pulses for the terminal side:
/twp = /host * /wr                          ; Terminal-Write-Pulse
/trp = /host * /rd                          ; Terminal-Read-Pulse

; Register read and write pulses for the host side:
/bwp = /biorq * /bwr * baseadr * /ba0       ; Bus-Write-Pulse
/brp = /biorq * /brd * baseadr * /ba0       ; Bus-Read-Pulse

; Status signals (R/S-Flip-Flops) for terminal (internal):
trxf = (/biorq * /bwr * baseadr * /ba0)     ; set TRXF at Bus-Write
   + trxf * /(/host * /rd                   ; hold until Terminal-Read
ttxe = (/biorq * /brd * baseadr * /ba0      ; set TTXE at Bus-Read
   + ttxe * /(/host * /wr                   ; hold until Terminal-Write

; Status signals for host (via bus D0 and D2);
bd0  = /ttxe                                ; BRXF: Data Host available
bd2  = /trxf                                ; BTXE: Terminal buffer free
bd0.trst = /biorq * /brd * baseadr * ba0
bd2.trst = /biorq * /brd * baseadr * ba0
```

6. Connector Pinouts

CN1 (ECB-Bus):

a	Nr	c
+5V	1	+5V
D5	2	D0
D6	3	D7
D3	4	D2
D4	5	A0
A2	6	A3
A4	7	A1
A5	8	
A6	9	A7
	10	
	11	IEI
	12	
	13	
	14	D1
	15	
	16	IEO
	17	
	18	
	19	
	20	
	21	
	22	/WR
	23	
	24	/RD
	25	
	26	/RESOUT
/IORQ	27	
	28	
	29	
	30	
	31	/RESIN
GND	32	GND

CN2 (MF2-Keyboard):

Signal	6-pin. MiniDIN	5-pin. DIN
Clock	5	1
Data	1	2
Ground	3	4
Vcc	4	5

CN3 (Hercules-Monitor):

1-5	Ground
6	Intensity
7	Video
8	Horizontal Sync.
9	Vertical Sync.

7. Software

The HGT uses two addresses in the I/O address space of the ECB-bus. The base address can be freely chosen by appropriate GAL programming (in steps of two). With the standard GAL contents, the addresses 60h and 61h are used. For the host, the registers appear as follows:

60h **Data Port**
Writing to the port outputs one byte of data to the terminal. Reading this port will get one data byte from the terminal.

61h **Status Port**
Reading this port gets the current interface status. Only two bits are used:

Bit 0 : Character from HGT available
Bit 2 : HGT ready to receive data

For those of you, who want to write their own software (or software extensions) for the HGT, here are some internal details.

Memory map of the Z80:

0000-3FFF	16k program memory (EPROM)
4000-7FFF	16k data memory (RAM)
8000-FFFF	32k screen memory

All of those areas are expandable by bank switching. When page mode EPROMs are used, page selection is done by writing the new page address to any address within the EPROM area (for details, see the manufacturer's data sheet). Switching banks of data and screen memory is done via the GPO port (see below). With all paging and bank switching, be extremely careful!

I/O map of the Z80 (16-bit-addressing!):

xx00	bus interface (read/write)
xx40	GPI port (status, keyboard, jumpers)
03Bx	hercules controller chip
xxCx	GPO port (fonts, keyboard, banks, speaker)

The input port is used as follows:

Bit 7 bus interface: buffer free to get a data byte
Bit 6 keyboard: clock signal
Bit 5 keyboard: data signal
Bit 4-0 jumpers J6-J2 (jumper set: bit = 0)

With the output port (GPO), accessing one of 16 possible addresses will reset or set a single output bit:

Address	Function
C0/C1	speaker off / on
C2/C3	font external (EPROM) / internal (HGC)
C4/C5	keyboard clock open / low
C6/C7	keyboard data open / low
C8/C9	screen memory bank 0/1
CA/CB	data memory bank 0/1
CC/CD	font selection address bit 1 0/1
CE/CF	font selection address bit 0 0/1

The hercules controller chip contains several registers, which are accesses via I/O addresses 03B4 to 03BF (caution: 16-bit addressing!):

03B4	6845 Index Register
03B5	6845 Data Register
03B8	Display Mode Control Port:
	Bit 7: 1 = Select Grafics Bank 1
	Bit 5: 1 = Text Blinker On (0 = Off)
	Bit 3: 1 = Screen Active (0 = Blank)
	Bit 1: 1 = Grafics Mode (0 = Text Mode)
03BA	Display Status Port:
	Bit 7: 1 = Active Display (0 = Vert. Retrace)
	Bit 3: 1 = Dots On (0 = Dots Off)
	Bit 0: 1 = Sync Active (Screen Blanked)
03BF	Display Configuration Register:
	Bit 1: 1 = Allow Bank 1 Selection
	Bit 0: 1 = Allow Grafics Mode

Besides these registers, there are some more covering light-pen and printer support, but those functions are not supported by the HGT hardware.

The various registers of the CRTC 6845 (inside the HGC) which generates the complete video timing, are accessed by an index register and a data register. Before accessing the data register, the appropriate register address must be written to the index register. The CRTC contains the following registers:

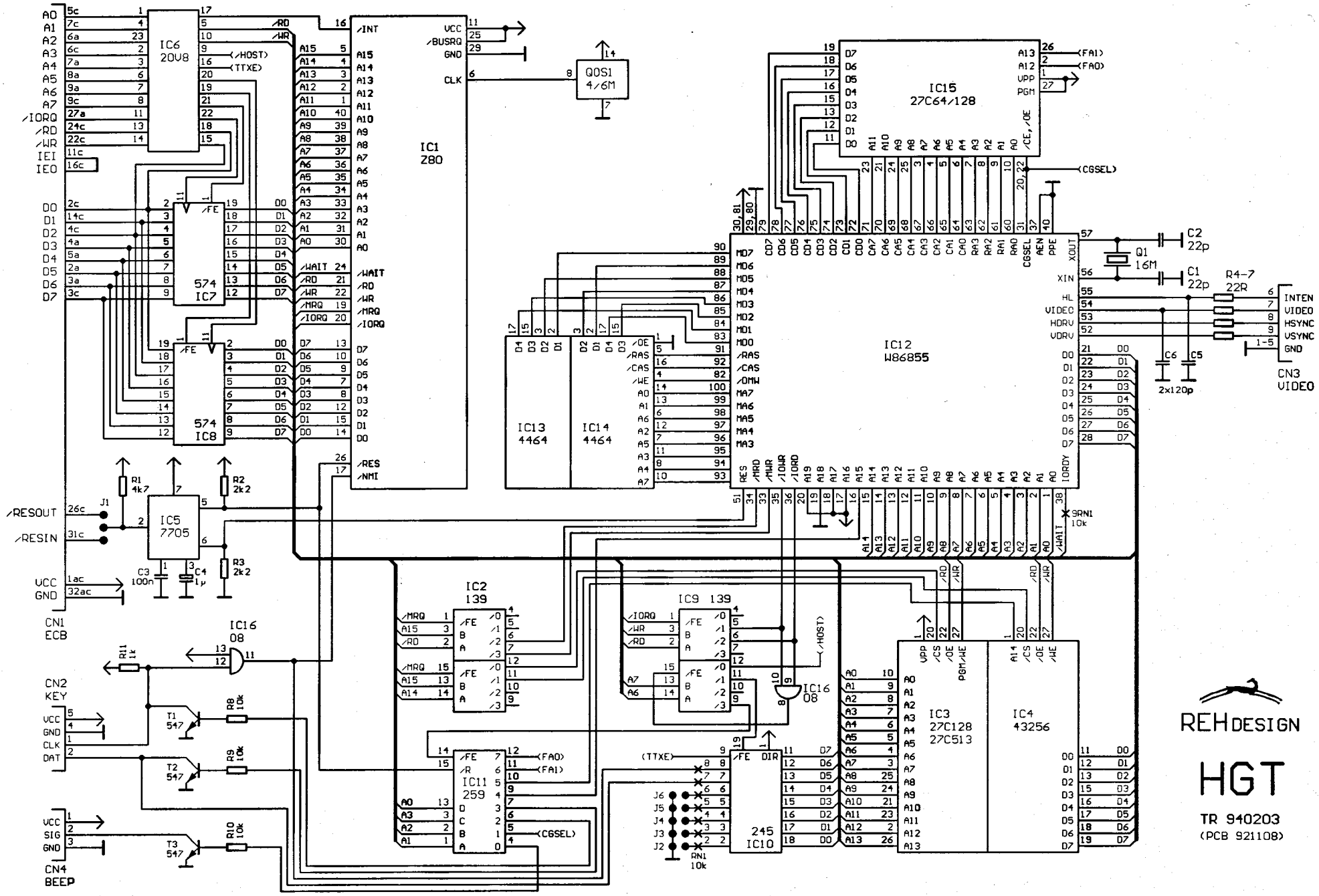
Index	Register Contents
0	characters per line total, incl. blanking, -1
1	visible characters per line
2	character number for sync start, -1
3	sync length in characters, -1
4	total complete lines , incl. blanking, -1
5	additional pixel rows per screen
6	visible lines
7	line number for sync start, -1
8	mode register (always 2)
9	pixel rows per line, -1
10	pixel row for cursor start
11	pixel row for cursor end
12	display start address (high), always 0
13	display start address (low), always 0
14	cursor position (high)
15	cursor position (low)

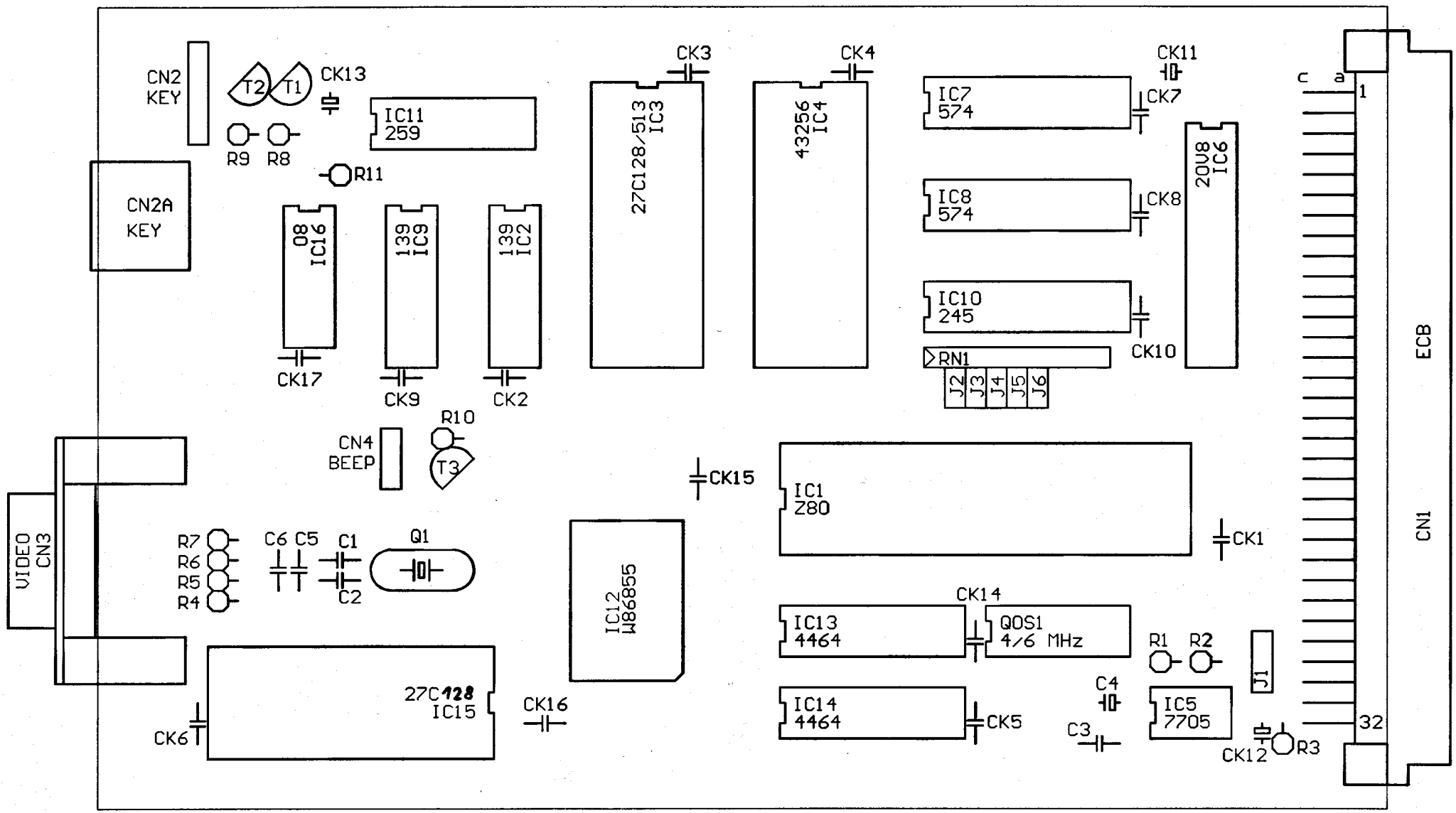
One "character" is always 9 pixels wide in text mode, and 16 pixels wide in grafics mode. One "line" is normally 14 pixel rows in text mode, and 4 pixel rows in grafics mode. Line height can be programmed to a different value in text mode, but not in grafics mode. For compatibility reasons (PC shit!) the HGC limits the addressable screen memory in text mode to 2048 visible characters, so screen formats larger than the usual 80 by 25 characters are impossible.

When programming the CRTC registers, care must be taken to not exceed the specified limits of the horizontal and vertical frequencies of the monitor. For Hercules type monitors, the horizontal frequency is nominal 18.4 kHz and the vertical frequency is nominal 50 Hz.

In text mode, two data bytes are stored in the screen memory for each character position. The first byte contains the character code, while the second byte defines the attributes of that character. Screen memory addresses increment continuously from left to right within each line, and from top to bottom of the screen. Screen memory addressing in grafics mode is rather complex, so it is not explained here. For details, read the common literature (i.e. PC magazines).

The external fonts stored in the EPROM contain 16 byte per character, with each byte representing a pixel row (8 pixels in horizontal direction), from top to bottom of the character. The most significant bit (bit 7) is the leftmost pixel. The HGC inserts a blank pixel between each two characters, so the character cell is truly 9 pixels wide, and the font itself need not contain margins. However, to support block grafics using the special PC characters, there is an exception: if the character code is within C0h to DFh, the rightmost pixel of the font is repeated instead of the usual blank pixel.


IC1
Z80
IC2
139
IC3
27C128
27C513
IC4
43256
IC5
7705
IC6
20U8
IC7
574
IC8
574
IC9
139
IC10
245
IC11
259
IC12
W86855
IC13
4464
IC14
4464
IC15
27C64/128
IC16
08
IC16
08
Q0S1
4/6M
Q1
16M
C1
22p
C2
22p
C3
100n
C4
1µ
C5
C6
2x120p
R1
4k7
R2
2k2
R3
2k2
R4-7
22R
R8
10k
R9
10k
R10
10k
R11
1k
RN1
10k
9RN1
10k
T1
547
T2
547
T3
547
CN1
ECB
CN2
KEY
CN3
VIDEO
CN4
BEEP
J1
J2
J3
J4
J5
J6
/RESOUT
/RESIN
VCC
GND
/INT
/BUSRQ
/RES
/NMI
/WAIT
/RD
/WR
/MRQ
/IORQ
/HOST
/TTXE
/CGSEL
/FA0
/FA1
INTEN
VIDEO
HSYNC
VSYNC
REHDESIGN
HGT
TR 940203
(PCB 921108)



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